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HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
SPITTLE, MATTHEW D	
ART UNIT	**PAPER NUMBER**
2111	

DATE MAILED: 01/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/829,057	SHAVER ET AL.	
	Examiner	Art Unit	
	Matthew D. Spittle	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/21/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities: Page 5, lines 16 – 24 reference the motherboard as Figure 1, item 102. Figure 1 lists item 102 as the chassis.

Page 8, lines 16 – 20 describes USB cable 502 connecting USB header 422 with USB header 212, and USB cable 504 connecting USB header 424 with USB header 210. Figure 5 shows that numbering of USB cables 502 and 504 is reversed.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 8 – 11, 15, 18 – 21, and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Lelong et al

With regard to claim 1, Lelong et al. describe a system for providing an Internal Universal Serial Bus (USB) port within a computer chassis, the computer chassis

internally mounting a motherboard having a first USB header for communicating with an external USB port, said system comprising:

A printed wire board (PWB) (paragraph 38; Figure 2, item 104) supporting a second USB header (paragraph 38; Figure 2, item 103), a third USB header (paragraph 38; Figure 2, item 101), a USB hub (paragraph 40) and the internal USB port (paragraph 39; Figure 2, item 102), the PWB being mountable at a location within the computer chassis (Paragraph 19 describes the PWB plugging into the USB header. Examiner recognizes that the header itself provides the mounting function for the card.)

The second USB header operative to communicate with the first USB header (paragraph 40 describes a connector (Figure 2, item 103) adapted to connect with the motherboard USB header socket (interpreted as the first USB header).

The third USB header operative to communicate with the external USB port (Figure 2, item 14 shows a cable connecting the third USB header to the external USB port (interpreted as a USB front connection)).

A USB hub operative to communicative information to and from the first USB header of the motherboard via the second USB header, and to communicate information to and from the external USB port via the third USB header (paragraphs 15,16, 40);

The internal USB port being operative to communicate information to and from the motherboard via the USB hub (paragraphs 15, 16, 40).

With regard to claim 2, Lelong et al. describe the system of claim 1, wherein the location at which the PWB is mounted is a location other than a Peripheral Component Interface PCI) expansion slot of the computer chassis (paragraph 40 describes a connector adapted to connect the PWB to a motherboard USB header socket; paragraph 39 describes the PWB being implemented in a cable form-factor).

With regard to claim 8, Lelong et al. describe the system of claim 1 further comprising:

A first USB cable operative to connect the first USB header of the motherboard with the second USB header (paragraph 39 describes the PWB device comprising a cable form-factor. Examiner interprets this as meaning that the PWB device would connect via a cable between the first USB header (on a motherboard) and a second USB header on the PWB device itself).

A second USB cable operative to interconnect the third USB header with the external USB port (Figure 2, item 14 shows a cable connecting an external USB port with the third USB header).

With regard to claim 9, Lelong et al. describe a computer system comprising:

A chassis defining an interior (Figure 2, item "Chassis");

A first Universal Serial Bus (USB) port externally mounted to the chassis (Figure 2, item 13);

A motherboard mounted within the interior of the chassis, the motherboard having a first USB header for communicating with the first USB port (Figure 2, item "Motherboard"; Figure 2, item "USB header");

A daughter card mounted within the interior of the chassis (Figure 2, item 100), the daughter card communicating with the motherboard and having a second USB port (Figure 2, item 102), a USB hub (paragraphs 15, 16, 40), a second USB header (Figure 2, item 103), and a third USB header (Figure 2, item 101);

The USB hub being operative to communicate information to and from the first USB header of the motherboard via the second USB header of the daughter card, and to communicate information to and from the first USB port via the third USB header of the daughter card (paragraphs 15, 16, 40 describe communicating between the ports using the USB hub);

The internal USB port being operative to communicate information to and from the motherboard via the USB hub and the second USB header of the daughter card (paragraphs 15, 16, 40);

With regard to claim 10, Lelong et al. describe the system of claim 9, wherein:

The chassis has a Peripheral Component Interface (PCI) expansion slot (Figure 2, item 16);

The daughter card is mounted at a location other than the expansion slot (Figure 2 shows item 100 being mounted to the motherboard; paragraphs 40, 41).

With regard to claim 11, Lelong et al. describe the system of claim 9, wherein the motherboard controls continuity of power to the daughter card (Paragraph 40 describes the USB management circuit being powered via the USB bus. Examiner interprets the USB bus to be stemming from the motherboard, and therefore meets this limitation).

With regard to claim 15, Lelong et al. describe the system of claim 9, further comprising:

Means for securing the daughter card to the chassis (paragraphs 39 and 40 describe the PWB taking card form-factor or cable form-factor, wherein both are mounted by being attached to the motherboard header (Figure 2, item 103)).

With regard to claim 18, Lelong et al. describe the system of claim 1 further comprising:

A first USB cable operative to connect the first USB header of the motherboard with the second USB header (paragraph 39 describes the PWB device comprising a cable form-factor. Examiner interprets this as meaning that the PWB device would connect via a cable between the first USB header (on a motherboard) and a second USB header on the PWB device itself).

A second USB cable operative to interconnect the third USB header with the external USB port (Figure 2, item 14 shows a cable connecting an external USB port with the third USB header).

With regard to claim 19, Lelong et al. describe a system for providing an internal Universal Serial Bus (USB) port within a computer chassis, the computer chassis internally mounting a first USB header for communicating with an external USB port, said system comprising:

A printed wire board (PWB) (Figure 2, item 100) supporting a USB hub (paragraphs 15, 16, 40) and a USB port (Figure 2, item 101), the PWB being operative to provide passthrough communication between the first USB header (Figure 2, item 103) and the external USB port (Figure 2, item 13), the PWB being internally mountable within a computer chassis such that the USB port of the PWB operates as an internal USB port (paragraphs 39 and 40 describe the PWB taking card form-factor or cable form-factor, wherein both are mounted by being attached to the motherboard header (Figure 2, item 103)).

With regard to claim 20, Lelong et al. describe a system for providing an internal Universal Serial Bus (USB) port within a computer chassis, the computer chassis internally mounting a first USB header for communicating with an external USB port, said system comprising:

Means for providing passthrough communication between the first USB header and the external USB port (Figure 2, item 14 shows a cable connecting the USB header of the motherboard with an external USB port (item 13)), the means for providing pasthrough communication being internally mountable within a computer chassis such that, when mounted therein (paragraphs 39 and 40 describe the PWB taking card form-

factor or cable form-factor, wherein both are mounted by being attached to the motherboard header (Figure 2, item 103)), the means for providing passthrough communication additionally provides the internal USB port (Figure 2, item 102) within the computer chassis.

With regard to claim 21, Lelong et al. describe a method for providing an internal Universal Serial Bus (USB) port within a computer chassis, said method comprising:

Providing a computer chassis (Figure 2, item "Chassis") having an external USB port (Figure 2, item 13) and an internally mounted first USB header (Figure 2, item "USB header") for communicating with the external USB port;

Providing a printed wire board (PWB) (Figure 2, item 100; paragraph 38) supporting a USB hub (paragraphs 15, 16, 40) and a USB port (Figure 2, item 102).

Internally mounting the PWB within the computer chassis (paragraphs 39 and 40 describe the PWB taking card form-factor or cable form-factor, wherein both are mounted by being attached to the motherboard header (Figure 2, item 103)), such that the PWB provides passthrough communication between the first USB header (Figure 2, item 103) and the external USB port (Figure 2, item 13), with the USB port of the PWB (Figure 2, item 102) operating as an internal USB port (paragraph 41).

With regard to claim 23, Lelong et al. describe the method of claim 21, wherein internally mounting the PWB within the computer chassis comprises:

Interconnecting a first USB cable between the first USB header and the PWB (paragraph 39 describes the PWB device comprising a cable form-factor. Examiner interprets this as meaning that the PWB device would connect via a cable between the first USB header (on a motherboard) and a second USB header on the PWB device itself);

Interconnecting a second USB cable between the PWB and the external USB port (Figure 2, item 14 shows a cable connecting an external USB port with the third USB header).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 3, 4, 5, 12, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lelong et al. in view of Schutz.

With regard to claims 3 and 12, Lelong et al. fail to describe a voltage regulator.

Schutz teaches a voltage regulator operative to receive a first voltage output from the motherboard and to provide, in response thereto, a second voltage output (column 2, lines 12 – 15).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the voltage regulator as taught by Schutz into the system of Lelong et al. for purposes of powering the USB hub. This would have been obvious since Schutz teach that many computer systems are designed around chips that require 5V, however, certain chips in the same system may require only 3.3V. Therefore, Schutz discloses a need to power 3.3V devices (such as a USB hub) in a 5V system (such as a motherboard).

With regard to claims 4 and 13, Schutz teaches the additional limitation wherein the first voltage output is approximately 5 volts, and the second voltage output is approximately 3.3 volts (column 2, lines 12 – 15).

With regard to claims 5 and 14, Lelong et al. implicitly teach the additional limitation wherein the PWB/daughter card is operative to receive a third voltage output from the motherboard (Lelong et al. teach an external USB port. According to the USB specification, USB devices can be powered over the bus (page 17, section 4.2.1). Since the motherboard is providing the power to the PWB through the motherboard header socket (Figure 2, item 103), and the PWB then providing power to the external USB port via a cable (Figure 2, item 14), this limitation is met).

* * *

Claims 6, 7, 16, 17, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lelong et al. in view of Le et al.

With regard to claims 6 and 16, Lelong et al. fail to teach a chassis having mounts or the PWD having apertures.

Le et al. teach the chassis (Figures 3A, 3B, item 100) having mounts extending into the interior thereof (Figures 3A, 3B; items 333, 334);

The PWB has apertures formed therethrough, each of the apertures being operative to receive one of the mounts such that insertion of the mounts into ths

apertures secures the PWB to the chassis (where the PWB is interpreted in Figures 3A and 3B as item 220, and the apertures are interpreted as mounting holes (item 221).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the mounting means as taught by Le et al. into the system of Lelong et al. for the purpose of mounting the PWB in a secure manner to the chassis.

With regard to claims 7 and 17, Le et al. teach the additional limitation wherein the mounts form interference fits with the apertures when the mounts are inserted within the apertures (Figure 3A and 3B clearly show an interference fit between the mounts (items 333, 334) and the apertures (item 221)).

With regard to claim 22, Le et al. teach the additional limitation wherein:

The computer chassis (Figures 3A, 3B, item 100) has mounts extending into the interior thereof (Figures 3A, 3B; items 333, 334);

The PWB has apertures formed therethrough (where the PWB is interpreted in Figures 3A and 3B as item 220, and the apertures are interpreted as mounting holes (item 221);

Internally mounting the PWB within the computer chassis comprises inserting the mounts into the apertures to secure the PWB to the computer chassis (paragraph 22 describes aligning the aperture (mounting hole) with the mount (standoff) and pressing

the two together. Conversely, applying upward pressure releases the PWB from the chassis).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Spittle whose telephone number is (571) 272-2467. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MDS

Khanh Dang
Primary Examiner